forming a conductive capping layer overlying the plurality of support structures, wherein the conductive capping layer electrically contacts the bond pad.

REMARKS

Claims 1, 8, and 24 have been amended to more clearly define the present invention and claim 32 has been added. Applicants submit the amendment does not add new matter to the current Application.

Claim Rejection - 35 USC §102

Applicants submit that claims 1-5, 10, 24-28 and 30 are not anticipated under 35 U.S.C. 102(b) by U.S. Patent No. 5,149,674 (Freeman). Claims 1 and 24 have been amended to more clearly define the present invention by including limitations that specify that the vias that interconnect the bond pad interconnect level (uppermost interconnect level) to the underlying interconnect level (first interconnect level) are positioned outside/beyond regions below the bond pad. Applicants submit that support for this limitation can be found on page 8, line 28 through page 9, line 2 of Applicants' specification and in Applicants' FIG. 2. This is in contrast to Freeman which teaches a bond pad wherein alternating interconnect and via levels are formed overlying each other such that the bond pad electrically/physically connects to an underlying regions by way of vias directly below the bond pad. Applicants submit that because the interconnecting vias disclosed in claims 1 and 24 are not positioned below the bond pad, claims 1 and 24 cannot anticipate Freeman. Applicants further submit that claims 2-5, 10, 25-28, and 30, which depend either directly or indirectly from the base claims 1 and 24 are allowable for at least those reasons that make claims 1 and 24 allowable. Accordingly, withdrawal of the anticipation rejection is respectfully requested.

Applicants disagree with the Office Action's position that Freeman anticipates claim 3 and submit that rejection of claim 3 was improper. In response, claim 32 has been added. Claim 32 is simply claim 3 rewritten in independent form to include the limitations from base claim 1. Freeman does not teach the formation of dielectric studs and as a result, Freeman cannot teach formation support structures overlying dielectric studs. Accordingly, Applicants submit that the rejection of claim 3 (now claim 32) was improper and respectfully request that it be withdrawn.

Claim Rejection - 35 USC §103

In view of Applicants' amendment to independent claims 1 and 24, Applicants submit that the Freeman reference does not support an obviousness rejection under 35 U.S.C. 103(a). Applicants therefore submit that: (1) claim 6 is not obvious over Freeman as applied to claims 1-5, 10, 24-28, and 30, and further in view of U.S. Patent No. 4,723,197 (Takiar); (2) claims 8, 9, 29, and 31 are not obvious over Freeman as applied to claims 1-5, 10, 24-28 and 30, and further in view of U.S. Patent No 5,942,448 (White); and (3) claim 11 is not obvious over Freeman as applied to claims 1-5, 10, 24-28, and 30 and further in view of U.S. Patent No 5,912,510 (Hwang). Accordingly, withdrawal of the obviousness rejection of claims 6, 8, 9, 29, 31 and 11 is respectfully requested.

Respectfully submitted,

SEND CORRESPONDENCE TO:

Motorola, Inc.
Law Department

Customer Number: 23125

By: _____
Robert A. Rodriguez
Agent of Record
Reg. No.: 45,049
Telephone: (512) 996-6839
Fax No.: (512) 996-6854
Email:

AMENDED CLAIMS SHOWING CHANGES MADE

1. (Amended) A method of forming a semiconductor device, comprising:

forming a first interconnect level over a semiconductor substrate;

forming an uppermost interconnect level that includes an interconnect portion and a bond pad over [an uppermost interconnect level over a semiconductor substrate] the first interconnect level, wherein:

[the uppermost interconnect level includes an interconnect portion and a bond pad;]

the interconnect portion contacts the first interconnect level by way of vias through an interlevel dielectric layer, and wherein all vias interconnecting the interconnect portion and the first interconnect level are positioned outside regions directly below the bond pad;

forming a passivation layer over the uppermost interconnect level;

removing portions of the passivation layer, wherein removing portions of the passivation layer exposes portions of the bond pad and forms a plurality of support structures overlying the uppermost surface of the bond pad; and

forming a conductive capping layer overlying the plurality of support structures, wherein the conductive capping layer electrically contacts the bond pad.

8. (Amended) The method of claim 1, further comprising forming a barrier layer between the capping layer and the bond pad, wherein the barrier layer overlies the support structures and abuts exposed portions of the bond pad [excluded by the support structures].

24. (Amended) A method of forming a semiconductor device, comprising:

depositing a dielectric layer over a semiconductor substrate;

patterning and etching a trench opening within the dielectric layer;

depositing a copper layer over the dielectric layer and within the trench opening;

removing portions of the copper layer not contained within the trench opening to define an uppermost interconnect level comprising a copper bond pad and an interconnect portion, wherein the interconnect portion physically couples to an underlying interconnect level by way of vias, wherein the vias are positioned beyond regions directly below the copper bond pad;

forming a passivation layer over the uppermost copper bond pad;

patterning and etching the passivation layer to define openings and support structures overlying the uppermost copper bond pad;

depositing a conductive layer over the support structures and within the openings, wherein the conductive layer electrically contacts the uppermost copper bond pad;

patterning and etching the conductive layer to define a capping film over the support structures and the openings.

32. (Added) A method of forming a semiconductor device, comprising:

forming an uppermost interconnect level over a semiconductor substrate, wherein the uppermost interconnect level includes an interconnect portion and a bond pad, wherein the bond pad has dielectric studs disposed within the bond pad;

forming a passivation layer over the uppermost interconnect level;

removing portions of the passivation layer, wherein removing portions of the passivation layer exposes portions of the bond pad and forms a plurality of support structures overlying the uppermost surface of the bond pad, wherein at least a portion of a support structure overlies a portion of a dielectric stud; and

forming a conductive capping layer overlying the plurality of support structures, wherein the conductive capping layer electrically contacts the bond pad.